**Laboratory Report Cover Sheet**

**18ECE206J ADVANCED DIGITAL SYSTEMS DESIGN**

**Fourth Semester, 2021-22 (Even semester)**

SRM Institute of Science and Technology College of Engineering and Technology

Department of Electronics and Communication Engineering

**Name :**

**Register No. :**

**Day/ Session :**

**Venue :**

**Title of Experiment :**

**Date of Conduction :**

**Date of Submission :**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks**  **Obtained** |
| Pre lab and Post lab | 10 |  |
| Lab Performance | 20 |  |
| Simulation and results | 10 |  |
| Total | 40 |  |

**REPORT VERIFICATION**

**Staff Name : Signature :**

## 10. Implementation of Multiplexers and DE-Multiplexers

**Aim**: To design 4X1 multiplexers and 1X4 de-multiplexers using VHDL.

Components required; Xilinx ISE &ModelSim

##### Theory

In electronics, a **Multiplexer** (or **MUX**), also known as a **data selector**, is a device that selects between several analog or digital input signals and forwards it to a single output line. A multiplexer of inputs has select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. Multiplexers can also be used to implement Boolean functions of multiple variables.

An electronic multiplexer makes it possible for several signals to share one device or resource, for example, one A/D converter or one communication line, instead of having one device per input signal.

Conversely, a **Demultiplexer** (or **Demux**) is a device taking a single input and selecting signals of the output of the compatible **mux**, which is connected to the single input, and a shared selection line. A multiplexer is often used with a complementary Demultiplexer on the receiving end.

An electronic multiplexer can be considered as a multiple-input, single-output switch, and a demultiplexer as a single-input, multiple-output switch. The schematic symbol for a multiplexer is an isosceles trapezoid with the longer parallel side containing the input pins and the short parallel side containing the output pin. The schematic and logic diagram for 4-to-1 multiplexer are shown in the below figure.

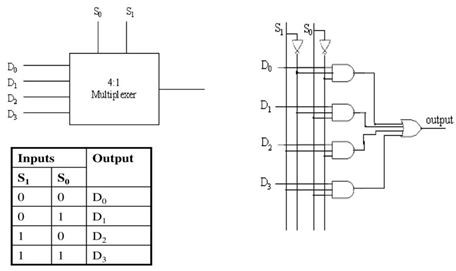


Fig.1 Block diagram, Truth table and Logic diagram of 4X1 Multiplexer

**VHDL Code for 4:1 Mux:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity mux\_4to1 is port(

D0,D1,D2,D3 : in STD\_LOGIC; S0,S1: in STD\_LOGIC;

Y: out STD\_LOGIC );

end mux\_4to1;

architecture behavioral of mux\_4to1 is begin

process (D0,D1,D2,D3,S0,S1) is begin

if (S0 ='0' and S1 = '0') then

Y <= D0;

elsif (S0 ='1' and S1 = ‘1’) then

Y <= D1;

elsif (S0 ='0' and S1 = '1') then

Y<= D2;

else

Y <= D3;

end if;

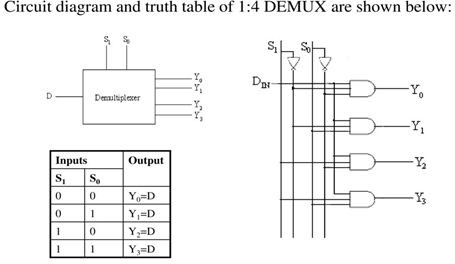
end process; end behavioral;

Fig.2 Block diagram, Truth table and Logic diagram of 1X4 DeMultiplexer

**VHDL Code for 1:4 Demux:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity demux\_1to4 is

port( D : in STD\_LOGIC; S0,S1: in STD\_LOGIC;

Y0,Y1,Y2,Y3: out STD\_LOGIC);

end demux\_1to4;

architecture behavioral of demux\_1to4 is begin

process (D,S0,S1) is begin

if (S0 ='0' and S1 = '0') then Y0 <= D;

elsif (S0 ='1' and S1 = '0') then Y1 <= D;

elsif (S0 ='0' and S1 = '1') then Y2 <= D;

else

Y3 <= F;

end if;

end process; end behavioral;

Pre-lab questions

1. What are the applications of multiplexer and de-multiplexer?
2. What is difference between decoder and de-multiplexer?
3. What is sequential statement in VHDL? List out the sequential statements.
4. Write the VHDL code for 2:1 multiplexer using case statement.

Post-lab questions

1. Write the VHDL code for 8:1 multiplexer using 4:1 multiplexer

2. Write the VHDL code for 1:8 de-multiplexer using behavioral model

3. Implement this F(A,B,C,D) = ∑m(0, 1,3, 4, 8, 9, 15) using suitable multiplexer

Result: